

57. (New) A device comprising:

- a package module sized to be interchangeable with standard package sizes;
- a graphics-processing die directly attached to the package module, the graphics-processing die encapsulated on the package module in a structure having a planar top surface; and
- a packaged memory die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the package module.

58. (New) A multi-die module, comprising:

- a substrate having a first surface and a second surface;
- an unpackaged semiconductor die mounted to the first surface of the substrate, the semiconductor die encapsulated in a structure having a planar top surface; and
- a packaged semiconductor die having a top surface and mounted on the first surface of the substrate; wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

59. (New) A multi-die module, comprising:

- a substrate having a first surface;
- an unpackaged semiconductor die mounted to the first surface of the substrate, the semiconductor die encapsulated in a structure; and
- a packaged semiconductor die mounted on the first surface of the substrate wherein the encapsulating structure is further comprised of an encapsulating material of a metal cap.

Please amend claims 2-6, 8, 9, 11, 16-18, 20, 23, 44-47, 53 and 54 as follows.

Sub
D1
2. (Amended) The device as in Claim 56, wherein the packaged semiconductor is packaged in a ball grid array package.

3. (Amended) The device as in Claim 56, wherein the unpackaged semiconductor die is a graphics-processor.

C2
4. (Amended) The device as in Claim 56, wherein the packaged semiconductor is a memory.

5. (Twice Amended) The device as in Claim 56, wherein a plurality of packaged semiconductors are attached to the package module.

D
6. (Twice Amended) The device as in Claim 56, wherein the unpackaged semiconductor die is wire bonded to the package module.

C3
8. (Amended) The device as in Claim 56, wherein attached includes surface-mount technology reflow.

9. (Thrice Amended) The device as in Claim 56, wherein the encapsulated structure has a footprint greater than the footprint of the unpackaged semiconductor die.

C4
11. (Amended) The device as in Claim 56, wherein the footprint size of the package module is one of 35mm X 35mm, 31mm X 31mm, 27mm X 27mm, 37.5mm X 37.5mm, 40mm X 40mm, 42mm X 42mm, or 42.5mm X 42.5mm.

C5
16. (Amended) The device as in Claim 56, wherein the packaged memory is packaged in a ball grid array package.

SUB 17
C5
17. (Twice Amended) The device as in Claim 57, wherein a plurality of packaged memory are attached to the package module.

18. (Twice Amended) The device as in Claim 57, wherein directly attached includes the graphics processing die being wire bonded to the package module.

C6
20. (Amended) The device as in Claim 57, wherein attached includes surface-mount technology reflow.

C7
23. (Amended) The device as in Claim 57, wherein the standard package sizes include one of 35mm X 35mm, 31mm X 31mm, 27mm X 27mm, 37.5mm X 37.5mm, 40mm X 40mm, 42mm X 42mm, or 42.5mm X 42.5mm.

44. (Amended) The multi-die module as in Claim 58, further including a second packaged semiconductor die mounted on the first surface of the substrate.

C8
45. (Amended) The multi-die module as in Claim 58, further including a plurality of unpackaged semiconductor die mounted on the first surface of the substrate.

46. (Amended) The multi-die module as in Claim 58, wherein the unpackaged semiconductor die is mounted to the first surface of the substrate by wire bonding.

47. (Amended) The multi-die module as in Claim 58, wherein the encapsulating structure is further comprised of an encapsulating material including epoxy, metal cap or silicon coatings.

C9
53. (Amended) The multi-die module as in Claim 58, wherein the unpackaged semiconductor die is a graphics processor.